Application No.: 09/849,530 Docket No.: 20136-00344-US

REMARKS

Claims 15-30 are now in the application. The indication that claims 19 and 22-25 contain allowable subject matter is hereby noted with appreciation.

Claims 15, 29 and 30 have been amended to recite "poorly adherent" in place of "does not adhere well" for purposes of clarification and not to further restrict the scope of these claims. Claim 15 has also been amended by deleting the term "the steps of" which is deemed to be superfluous.

Claim 28 has been amended to correct its dependency for purposes of clarification.

The rejections of claims 15 and 28 under 35 U.S.C. §112, second paragraph have been overcome by the above amendments to the claims.

Claims 15, 16 and 26 were rejected under 35 U.S.C. §102 (e) as being anticipated by and claims 17, 18, 20, 21 and 27 were rejected as being obvious under 35 U.S.C. §103 (a) over U.S. Patent 6,143,657 to Liu et al. Claims 28-30 were rejected as being obvious under 35 U.S.C. §103 (a) over U.S. Patent 6,143,657 to Liu et al. in view of the Admitted State of the Art.

These rejections are not deemed tenable since 6,143,657 to Liu et al. is not prior art to the present invention.

In particular, attached hereto is an unsigned Declaration under 37 CFR 1.131 and attached exhibits which evidences that the present invention was conceived by the present inventors and reduced to practice in the U.S. by them and/or under their direction and/or supervision prior to January 4, 1999, the filing date of Liu et al. The fully executed Declaration will be filed when received by the undersigned.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Application No.: 09/849,530 Docket No.: 20136-00344-US

Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, under Order No. 20136-00344-US from which the undersigned is authorized to draw.

Dated: September 22, 2003

Respectfully submitted,

By _____

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IBM Confidential

Invention Disclosure FI898-0100

ethod for improving SI3N4 to Cu adhesion by copper germanide formation

le of Invention (Short & Descriptive)						
lethod for improving Si3N4 to Cu adhesion by copper germanide formation						
closure No. FI898-0100	Functional Manager B. DAVARI	Receiving Date	Receiving Time 21:54:36			
ent Attorney .P. ABATE	Evaluator J. RYAN - EM1	Evaluation Area 81				

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ble 1. Critical Dates Information

Date invention workable:	10/00/97
Used or Planned for product:	N
If so, Product Name?	
Release?	
Announce Date?	
ublic Demonstration or Use:	N
If so, When?	
Where?	
isclosed to Non-IBMers:	N
If so, When?	
Where?	
CDA in place?	
se in Manufacturing:	N
If so, When?	
Where?	
Product Name?	

EXHIBIT A

Problem

Silicon nitride is used as a passivation layer and as a copper diffusion barrier for copper-based interconnections in integrated circuits. Silicon nitride does not have strong adhesion to copper, however, and the nitride-to-copper interface is susceptible to delamination, especially under conditions of mechanical loading. Examples of instances where mechanical loading can lead to delamination include chemical-mechanical polishing steps during wafer processing, chip pull such as used in substrate rework, and removal of chips after burn-in from the temporary attach substrate.

Solution

It is proposed that the nitride-to-copper interface be removed by the formation of copper germanide at the surface of the copper interconnects. The copper germanide would preferably be formed by a process whereby germane (GeH_4) flows over the wafer at elevated temperature and reacts selectively with the copper wiring to form a germanide film. It is anticipated that nitride-to-germanide adhesion will be superior to nitride-to-copper adhesion similar to the adhesion improvement obtained by the formation of copper silicide. Although the selective formation of copper germanide and improved nitride adhesion are yet to be demonstrated, efforts to build the appropriate test structures at IBM are being pursued.

Evaluation Questions

Has this problem been solved before, how was it solved?

The formation of a copper silicide film on copper interconnects by flow of silane (SiH_4) at elevated temperature over a wafer with exposed copper wiring and selective reaction between silane and copper has been verified to eliminate nitride-to-copper adhesion problems. This invention has been patented by Motorola (US patent 5447887).

Why is your solution better?

Copper silicides have a relatively high electrical resistivity and may cause an unacceptably large increase in resistance of copper interconnects. Furthermore, copper silicides have been reported to be reactive with atmospheric oxygen and to suffer resistivity increases upon exposure to oxygen. Copper germanide on the other hand has been reported to have a much lower resistivity than copper silicide and is stable with regard to exposure to air.

Although selective formation of copper germanide is the preferred embodiment of this invention, the formation of a patterned copper germanide layer over copper wiring by blanket film deposition of copper germanide followed by conventional photolithographic and reactive ion etch processes is also possible.

Who outside of IBM (competitors) would want to use your solution?

Any semiconductor manufacturer employing copper interconnects would be interested in this solution.

How could IBM discover that competitors were using your solution?

Presence of copper germanide could detected by deconstruction analysis of competitor's products.

IBM Microelectronics — Logic BEOL

Method for Improving Si_3N_4 to Cu Adhesion by Copper Germanide Formation

V. McGahay, H. Nye, T. Ivers, J. Liu

Problem:

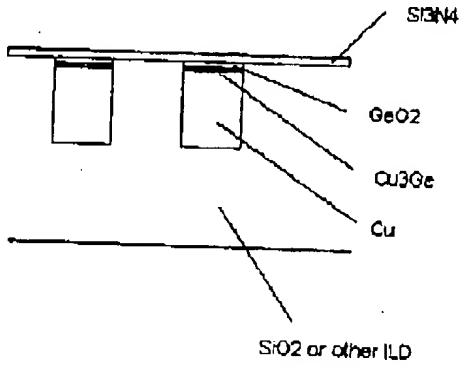
- Si_3N_4 is used as a Cu diffusion barrier and etch stop over every level of Cu metalization in CMOS7S
- adhesion of Si_3N_4 to Cu is marginal and has caused problems in CMOS7S
  - M2 nitride-to-copper delamination during M3 CMP of Cygnus
  - LM nitride pullout at C4 chip pull and chip shear
- improvement in the fundamentally poor nitride-to-copper adhesion is needed
- surface alloying copper in contact with nitride can improve adhesion
  - alloying step is preferably selective (i.e. requires no masking step)
  - increase in Cu resistivity should be minimal
- selective copper silicide formation has been found to eliminate LM nitride pullouts at C4 stud pull
  - silicide is formed by flowing SiH_4 over exposed copper
- copper silicide has several problems however
  - non-uniformity and non-repeatabilty of silicide formation has been observed
  - resistivity of Cu_3Si is high (55 $\mu\Omega$ cm vs. ~ 2.2 for Cu)
    - as silicided resistivity shift is ~15% for LM, 45% for Mx
  - subsequent thermal excursions of silicided copper results in additional resistivity shifts (~ 2x)
  - selective silicidation of copper has been patented by Motorola

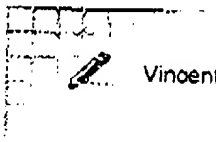
Solution:

- selective copper germanide formation to improve nitride-to-Cu adhesion
  - germanide formed by flowing GeH_4 over exposed copper
  - IBM held US patent 5420069 (Joshi et al.)
- advantages of copper germanide
  - very uniform and reproducible germanide formation compared to silicide in same reactor
  - relatively low resisitivity for Cu_3Ge (~5.5 $\mu\Omega$ cm at RT)
  - good adhesion to oxide (Liou et al., J. App. Phys. 77 (1995) 5443)
    - nitride adhesion to Cu_3Ge needs to be evaluated
  - possible Cu diffusion barrier (Aboelfotoh et al., Phys. Rev. B 44 (1991) 12742)
- disadvantage: resistivity increase upon thermal excursion similar to silicide
  - since resistivity is 1/10 that of silicide, may be able to tolerate the resisitvity increase
  - possible remedies
    - oxidation of thin Cu_3Ge to bind Ge into GeO_2
      - GeO_2 acts as an oxidation barrier for Cu (Liou et al., J. App. Phys. 77 (1995) 5443)
    - Cu_3Ge + Cu_3Si mixture?

Example Embodiment:

1. Form Cu wiring by single or dual damascene processing on a wafer
2. Flow GeH_4 over the wafer to form selectively a thin, continuous layer of Cu_3Ge
3. Expose wafer to an oxidizing environment to covert Ge in Cu_3Ge to GeO_2
4. Deposit nitride cap





Vincent McGahay
12:44 PM

To: Charles Davis/Fishkill/IBM@IBMUS
cc:
From: Vincent McGahay/Fishkill/IBM @ IBMUS
Subject: "IBM Confidential: 2Q98 Progress Report

2Q98 Progress Report

BEOL Insulators:

- qualification of Novellus Sequel Hex 408 as backup for 447 is complete for M1 - M4 (30% 7S wip, 40% 8S wip); qualification of remaining levels is in progress

C4:

- Lonestar DD2 open/short hardware was built and delivered for 7S T2 package qual
- Lonestar DD2 MQ-VQ-LM-TV-TD-FV, Sirocco LM-TV-TD-FV, and Opera M5-V5-LM-TV-TD-TV hardware was built and delivered for 7S T1 closure plan
- set up of selective oopper germanide capability for potential improvement of nitride adhesion on Hex 447 is in progress

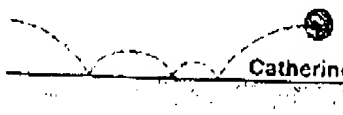
Wirebond:

- Sirius LM (1 lot) and MT (2 lots) hardware was built for G. Walker for electroless bond pad development

CMOS9S:

- Silk was chosen as upfront insulator for CMOS9S by low K taskforce
- performance and cost-of-ownership comparison of several different integration schemes for copper/low K was completed
- the low K integration team was organized for investigation of alternative integration options as well as continued investigation of dual damascene options
    - single damascene etchback scheme was chosen as a learning vehicle for alternative integration since it has several process steps which are common to the other alternatives considered
- hardware has been released for alternative integration builds
    - single damasscene etchback mechanical build completed through M2 test
    - dual damascene etchback build at M1/V1 Silk gapfill
    - through resist plate-up build at M1 ARC etch
- several dual damascene integration schemes are under consideration (standard, second hardmask, buried pattterned hardmask, bilayer hardmask); an effort to concentrate on standard dual damascene and reduce resource expenditure on alternatives is underway
- degradation of Silk electrical properties under bias/temperature stress on MOS structures which appears to be due to film defects was discovered; additional characterization is in progress
- two lots (3 wafers each) with TEOS and nitride caps, respectively, of Cygnus M1-TV-TD hardware were delivered to reliability engineering for investigation of Silk dielectric reliability in patterned copper structures

EXHIBIT C



02:08 PM

To: Henry Nye/Fishkill/IBM@IBMUS, Vincent McGahay/Fishkill/IBM@IBMUS, Thomas Ivers/Fishkill/IBM@IBMUS
cc:
From: Catherine Basa/Fishkill/IBM @ IBMUS
Subject: Status: 12T12E85L1,02
(4 wafer CuGe split)

Guys,

Since 12T12E85L1,02 (the 4 wafer lot with different CuGe thicknesses) is a child lot, there were some logistical difficulties getting it on the ASTC MCS2 system when it returned from BTV. Debbie Perez perservered, though, and the lot is at gate 840 - TV Final etch. However, inorder to overcome the logistical problems, the lot had to be renamed. The new lot name is 12T12E99L1,01.

The history of the lot's names is given below in case it is needed for future reference.

Original Lot Name	12T12E85L1, 02	4 Wafers
BTV Lot Name	XBT310004P, 01	4 Wafers
Current ASTC Lot Name	12T12E99L1, 01	6 Wafers (4 patterned + 2 Polyimide monitors)

Cathy

Basa@us.ibm.com IBM Microelectronics Division, East Fishkill, NY (914) 892-9831

EXHIBIT D